

Abstract

A fast-sensing amplifier for a flash memory comprised of a plurality of floating-gate memory devices and having a column line selectively coupled to the devices is disclosed. The column line is quickly discharged to ground before a read-biasing and
5 amplifying circuit quickly pulls up the line to the read-bias potential at a particular memory device. This potential is compared to a sense-reference potential by a differential amplifier within the fast-sensing amplifier. The binary state of the particular memory device is provided as the output of the fast-sensing amplifier.